Amendments to the Claims

1. (ORIGINAL) One-time programmable memory device comprising an MOS (metal-oxide semiconductor) selection transistor and an MOS memory transistor connected in series between a voltage supply line and ground, and further comprising programming means for applying voltages to a gate of said selection transistor, to a gate of said memory transistor and to said voltage supply line, which applied voltages force said memory transistor into a snap-back mode resulting in a current thermally damaging a drain junction of said memory transistor.

2. (ORIGINAL) One-time programmable memory device according to claim 1, wherein said programming means comprise means for first applying a predetermined voltage to said gate of said memory transistor and for then ramping down said predetermined voltage applied to said gate of said memory transistor until said memory transistor enters said snap-back mode.

3. (CURRENTLY AMENDED) One-time programmable memory device according to ~~claim 1 or 2~~claim 1, wherein said MOS transistors are NMOS (N-channel metal-oxide semiconductor) transistors.

4. (CURRENTLY AMENDED) One-time programmable memory device according to ~~one of the preceding claims~~claim 1, further comprising at least one resistor-capacitor unit arranged between a voltage supply and said gate of said selection transistor and between a voltage supply and said gate of said memory transistor, said resistor-capacitor unit ensuring that a predetermined voltage is applied to said gate of said selection transistor and said gate of said memory transistor at the earliest a predetermined time after powering up said one-time programmable memory device.

5. (CURRENTLY AMENDED) One-time programmable memory device according to ~~one of the preceding claims~~claim 1, wherein said programming means require a setup procedure for initiating their operation, which setup procedure

comprises more steps than applying one predetermined voltage level to said programming means.

6. (CURRENTLY AMENDED) One-time programmable memory device according to ~~one of the preceding claims~~claim 1, wherein said programming means apply a programming voltage to said voltage supply line which is higher than a voltage applied to said voltage line for other operations than thermally damaging a drain junction of said memory transistor.

7. (CURRENTLY AMENDED) One-time programmable memory device according to ~~one of the preceding claims~~claim 1, further comprising readout means for applying a high voltage to said gate of said selection transistor, for applying a low voltage to said gate of said memory transistor, for applying a readout voltage to said voltage supply line, for detecting a current through said transistors resulting with said applied voltages, for comparing said detected current with a predetermined current value, and for providing an indication that said memory transistor is programmed in case it is determined that said detected current exceeds said predetermined current value.

8. (CURRENTLY AMENDED) One-time programmable memory device according to ~~one of the preceding claims~~ claim 1 comprising a plurality of memory cells, each of said memory cells including a respective selection transistor and a respective memory transistor connected in series between said voltage supply line and ground, wherein said programming means are suited to apply voltages to said memory cells forcing any selected one of said memory transistors into a snap-back mode resulting in a current thermally damaging a drain junction of the respective memory transistor.

9. (CURRENTLY AMENDED) CMOS circuitry comprising a one-time programmable memory device according to ~~one of claims 1 to 8~~claim 1.

10. (ORIGINAL) Method for programming a one-time programmable memory, which memory comprises an MOS (metal-oxide semiconductor) selection transistor and an MOS memory transistor connected in series between a voltage supply line and ground, said method comprising applying voltages to a gate of said selection transistor, to a gate of said memory transistor and to said voltage supply line, which applied voltages force said memory transistor into a snap-back mode resulting in a current thermally damaging a drain junction of said memory transistor.